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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/701,185	BAO ET AL.	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: There is no support in the specification for the limitation of "a second substrate on said dielectric layer" as recited in claim 10. Appropriate correction is required.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the claimed limitation of "a second substrate on said dielectric layer" as recited in claim 10 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement

Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

4. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 7 recites, "the dielectric layer has a capacitance of at least about 5 nF/cm^{2}". A dielectric layer by itself has dielectric constant not a capacitance. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**

6. Claims 1-5, 12, 15 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Beuhler et al., US patent No. 6,342,164.

Regarding claim 1, Beuhler teaches (figs. 10-11) an apparatus comprising: a first substrate (26); a dielectric layer comprising a first dielectric material (10) on the first substrate (26), the dielectric layer having a dielectric layer thickness and being

traversed by through holes (11, pinholes) passing from an interface with the first substrate, to an opposite side of the dielectric layer; and a second dielectric material (col. 2, lines 60-65) (21) at least partially blocking the through holes.

Regarding claim 2, Beuhler teaches the entire claimed structure of claim 1 above including through holes having average diameters substantially smaller than an average spacing between mutually adjacent the through holes (11). The average diameters of the through holes (11) appears substantially smaller than the spacing between adjacent through holes.

Regarding claim 3, Beuhler teaches the entire claimed structure of claim 1 above including the second dielectric material (21) at least partially blocks a mutually adjacent pair of the through holes without forming a continuous layer between the mutually adjacent pair of through holes (refer to fig. 12).

Regarding claim 4, Beuhler teaches the entire claimed structure of claim 1 above including the dielectric layer (16) comprises pits (11, some of the pinholes can be considered pits) that produce surface roughness (pinholes seen microscopically give rise to surface roughness) in one surface of the dielectric layer, and wherein the second dielectric material (20) at least partially fills the pits in a manner that reduces the roughness.

Regarding claim 5, Beuhler teaches the entire claimed structure of claim 1 above including the dielectric layer (16) comprises bumps (region between adjacent pits 11 appear as a bump) on one surface thereof, and areas surrounding the bumps are at least partially smoothed with the second dielectric material (20 refer to fig. 12).

Regarding claim 12, Beuhler teaches (figs. 10-11) a method of making an apparatus comprising a first substrate (26) and a dielectric layer (10), comprising the steps of: providing a first substrate (26); providing a dielectric layer comprising a first dielectric (10) material on the first substrate (26), the dielectric layer having a dielectric layer thickness and being traversed by through holes (11, pinholes) passing from an interface with the first substrate, to an opposite side of the dielectric layer (10); and providing a second dielectric material (21) that at least partially blocks the through holes.

Regarding claim 15, Beuhler teaches the entire claimed structure of claim 12 above including the further step of providing a reaction initiator on the opposite side of the dielectric layer. Beuhler teaches a process of polymerization initiation (col. 2, lines 20-27) after forming the dielectric layer (10) in order to plug the pinholes/pits formed. Therefore Beuhler teaches reaction initiator on the opposite side of the dielectric layer.

Regarding claim 18, Beuhler teaches the entire claimed process of claims 4-5 and 12 above including dielectric layer comprises pits and bumps that produce surface roughness in one surface of the dielectric layer, and wherein the second dielectric material (21) at least partially fills the pits and at least partially smoothes areas surrounding the bumps in a manner that reduces the roughness.

7. Claims 1, 6, 12 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Srinivasan et al., US patent No. 5,731,235.

Regarding claim 1, Srinivasan teaches (figs. 1-4) an apparatus comprising: a first substrate (12); a dielectric layer comprising a first dielectric material (14) on the first

substrate (12), the dielectric layer having a dielectric layer thickness and being traversed by through holes (16, pinholes) passing from an interface with the first substrate, to an opposite side of the dielectric layer; and a second dielectric material (22) at least partially blocking the through holes.

Regarding claim 6, Srinivasan teaches the entire claimed structure of claim 1 above including the dielectric layer (14) thickness is within a range of between about 10 nanometers and about 5 microns (col. 3, lines 24-29).

Regarding claim 12, Srinivasan teaches (figs. 1-4) a method of making an apparatus comprising a first substrate (12) and a dielectric layer (14), comprising the steps of: providing a first substrate (12); providing a dielectric layer comprising a first dielectric (14) material on the first substrate (12), the dielectric layer having a dielectric layer thickness and being traversed by through holes (16) passing from an interface with the first substrate, to an opposite side of the dielectric layer (14); and providing a second dielectric material (22) that at least partially blocks the through holes.

Regarding claim 19, Srinivasan teaches (figs. 1-4) the entire claimed structure of claim 12 above including providing a dielectric layer produces a layer thickness within a range of between about 10 nanometers and about 5 microns (col. 3, lines 24-29).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan.

Srinivasan teaches the entire claimed structure of claim 1 above except explicitly stating that dielectric layer is capable of producing a capacitance of at least about 5 nF/cm2. However Srinivasan teaches the formation of a capacitor structure as illustrated in fig. 8.

Furthermore parameters such as capacitance in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristics during fabrication.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the spacing and area of the capacitor structure of Srinivasan to produce a capacitance as claimed in order to form a capacitance structure that is free of pinholes.

10. Claims 1, 8-13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dimitrakopoulos et al. US patent No. 5,981,970 in view of Beuhler.

Regarding claims 1 and 12, Dimitrakopoulos teaches (fig. 6) an apparatus and a method making an apparatus comprising: a first substrate (substrate) a dielectric layer comprising a first dielectric material (BST insulator) on the first substrate, the dielectric layer having a dielectric layer thickness.

Dimitrakopoulos does not teach the dielectric layer being traversed by through holes passing from an interface with the first substrate, to an opposite side of the

dielectric layer and a second dielectric material at least partially blocking the through holes.

Beuhler teaches dielectric layers such as BST (col. 2, lines 37-47) having through holes (pinholes 11) such as shown in figs. 10-12, and a second dielectric layer (21) partially blocking the through holes (fig. 12) in order to prevent shorts.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the dielectric layer taught by Beuhler in the structure of Dimitrakopoulos in order to prevent shorts.

Regarding claim 8, Dimitrakopoulos teaches (fig. 6) substantially the entire claimed structure of claim 1 above including a semiconductor layer (col. 6, line17-25).

Regarding claim 9, Dimitrakopoulos teaches (fig. 6) substantially the entire claimed structure of claim 1 above including the first substrate is a conductor (col. 6, lines 17-25).

Regarding claim 10, Dimitrakopoulos teaches (fig. 6) substantially the entire claimed structure of claim 1 above including a second substrate (gate) below the dielectric layer.

Regarding claim 11, Dimitrakopoulos teaches (fig. 6) substantially the entire claimed structure of claims 1 and 8 above including a source electrode (source) and a drain (drain) electrode in a spaced apart arrangement on the semiconductor layer (refer to fig. 6).

Regarding claim 13, Dimitrakopoulos teaches (fig. 6) substantially the entire claimed process of claim 12 above including the step of making the first substrate conductive while providing a second dielectric material (col. 6, lines 17-25).

Regarding claim 17, Dimitrakopoulos teaches (fig. 6) substantially the entire claimed process of claim 12 above including a semiconductor layer (col. 6, line17-25).

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beuhler.

Regarding claim 14, Beuhler teaches substantially the entire claimed process of claim 12 above except explicitly stating that a further step of providing a reaction initiator on the first substrate prior to providing the dielectric layer, wherein the providing of the dielectric layer does not deactivate a portion of the reaction initiator located near entrances of the through holes. However Beuhler teaches a process of polymerization initiation (col. 2, lines 20-27) after forming the dielectric layer (10) in order to plug the pinholes/pits formed where providing of the dielectric layer does not deactivate a portion of the reaction initiator located near entrances of the through holes.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the polymerization initiator taught by Beuhler before forming the dielectric layer in order to plug the pinholes/pits formed in the back side of the dielectric layer.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Srinivasan in view of Tickle US patent No. 4,420,497.

Srinivasan teaches substantially the entire claimed process of claim 12 above except explicitly stating the process further comprising the step of applying the second

dielectric material to the opposite side of the dielectric layer while an electrical field is applied to the first substrate.

Tickle teaches the process of using voltage source (electric field, refer to fig. 2 and also col. 3, lines 50-69 and col. 4, lines 1-27) in the method of plugging pinhole (13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the application of electric field taught by Tickle in the process of Srinivasan in order to expose more pinholes that will be filled during subsequent oxidation step.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
December 6, 2004

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